

CLAIMS

What is claimed is:

- 1 1. A method for testing cache performance of a processor design, the method
2 comprising:
3 searching a file that contains cache test results for a lot of wafers; and
4 determining at least one cache array location in at least one processor in the lot
5 wafers processor for which a cache test has failed.
- 1 2. The method of claim 1, wherein the searching the file comprises parsing the
2 file.
- 1 3. The method of claim 1, wherein the searching the file comprises opening the
2 file and parsing the file.
- 1 4. The method of claim 1, wherein the determining the at least one cache array
2 location comprises determining a column and row location in the corresponding cache
3 array.
- 1 5. The method of claim 1, further comprising developing a cache array repair
2 signature based on the at least one cache array location for which a cache test has
3 failed.
- 1 6. The method of claim 5, wherein the cache array repair signature defines a
2 cache array location associated with the processor design which has failed the cache
3 test in a statistically relevant percentage of the processors in the lot.

- 1 7. A system for testing cache performance of a processor design, the system
2 comprising:
3 a parser module for searching a file that contains cache test results for a lot of
4 wafers;
5 a composite repair failure identification module for determining cache array
6 locations for which a cache test has failed; and
7 a cache array repair signature module for determining at least one cache array
8 location associated with the processor design which has failed the cache test in a
9 statistically relevant percentage of the processors in the lot.
- 1 8. The system of claim 7, wherein the parser module is configured to open the
2 file that contains the cache test results.
- 1 9. The system of claim 7, wherein the parser module, the composite repair failure
2 identification module, and the cache array repair signature module comprise software
3 that is executed by a processor.
- 1 10. The system of claim 7, wherein the cache array repair signature module is
2 configured to determine a column and row location in the corresponding cache array.

1 11. A cache yield analysis program embodied in a computer-readable medium, the
2 program comprising:

3 logic configured to search a file that contains test results for a lot of wafers and
4 determine cache array locations for processors in the lot for which a cache test has
5 failed; and

6 logic configured to determine a cache array repair signature that defines at
7 least one cache array location associated with the processor design which has failed
8 the cache test in a statistically relevant percentage of the processors in the lot.

1 12. The program of claim 11, wherein the logic configured to determine a cache
2 array repair signature is further configured to determine a column and row location in
3 the corresponding cache array.

- 1 13. A system for testing cache performance of a processor design, the system
- 2 comprising:
- 3 means for searching a file that contains test results for a lot of wafers;
- 4 means for determining cache array locations for processors in the lot for which
- 5 a cache test has failed; and
- 6 means for generating a cache array repair signature that defines at least one
- 7 cache array location associated with the processor design which has failed the cache
- 8 test in a statistically relevant percentage of the processors in the lot.